What is claimed is:

1. An information-handling system, comprising:

a plurality of processing elements; and

one or more memory sections, wherein each memory section comprises:

a memory array having a plurality of locations;

a memory interface operatively connecting the memory array to each of the processing elements; and

a plurality of processor translation look-aside buffers, wherein each processor translation look-aside buffer is operatively coupled to the memory array and to one of the processing elements in order to translate addresses received from the processing elements, and wherein each processor translation look-aside buffer has a plurality of entries, each one of the plurality of entries being used to map a processor address into a memory array address of the memory array.

2. The information-handling system of claim 1, wherein the memory interface includes a FIFO, wherein the FIFO accepts memory commands from one or more of the processing elements and transmits each of the memory commands to at least one of the processor translation look-aside buffers.

3. The information-handling system of claim 1, wherein the memory interface includes a plurality of FIFOs, wherein each FIFO is associated with one of the processing elements, and wherein each FIFO accepts memory commands from its associated processing element and transmits the memory commands to one of the processor translation look-aside buffers.

4. The information-handling system of claim 1, wherein the memory sections further include one or more I/O translation look-aside buffers, wherein each I/O translation look-aside buffer is operatively coupled to the memory array and to one of the processing elements to translate addresses received from the processing element, and wherein each of the I/O translation look-aside buffers has a plurality of entries, each of the entries being used to map an I/O address into a memory array address of the memory array.

5. A method for addressing a memory within a memory system comprising:

routing a first memory command within the memory system, wherein the first memory command includes a first processor address;

mapping the first processor address into a first memory address using a mapping function associated with a first processor;

addressing memory data within the memory system with the first memory address;

routing a second memory command within the memory system, wherein the second memory command includes a second processor address;

mapping the second processor address into a second memory address using a mapping function associated with a second processor; and

addressing memory data within the memory system with the second memory array address.

6. The method of claim 5, wherein the routing of the first memory command includes processing the first memory command on a first in first out basis with regard to other memory commands.

7. The method of claim 5, wherein the second processor is an I/O processor.

8. An information-handling system comprising:

a memory; and

a plurality of processing elements, wherein each of the processing elements is operatively coupled to the memory,

wherein the memory includes mapping means for mapping processor addresses received from the processing elements into memory addresses in the memory, and wherein the mapping means includes a first mapping function for translating processor addresses associated with a first processing element and a second mapping function for translating processor addresses associated with a second processing element.

9. An information-handling system, comprising:

a plurality of processing elements; and

a memory having a first memory section, wherein the first memory section is operatively coupled to each processing element, and wherein the first memory section comprises:

a memory array;

a memory interface operatively connecting the memory array to each of the processing elements; and

a block transfer engine operatively coupled to the memory array, wherein the block transfer engine operates under command of one of the processing elements to transfer data from a memory location that cannot be addressed by the processing element to a memory location that can be addressed by the processing element.

10. The information-handling system of claim 9, wherein the memory interface includes a FIFO, and wherein the FIFO accepts block transfer commands from one or more of the processing elements and transmits the block transfer commands to the block transfer engine.

11. The information-handling system of claim 10, wherein the first memory section further includes a processor translation look-aside buffer associated with each processing element, and wherein each processor translation look-aside buffer has a plurality of entries, each of the entries being used to map a processor address received from its associated processing element into a memory array address within the memory array.

12. The information-handling system of claim 9, wherein the memory interface includes a plurality of FIFOs, wherein each FIFO is associated with one of the processing elements, and wherein each FIFO accepts block transfer commands from its associated processing element and transmits the block transfer commands to the block transfer engine.

13. The information-handling system of claim 9, wherein the first memory section further includes a plurality of processor translation look-aside buffers that are each operatively coupled to the memory array, wherein each of the processor translation look-aside buffers is associated with each of the processing elements, and wherein each of the processor translation look-aside buffers has a first plurality of entries, each of the first plurality of entries being used to map a processor address into a first memory array address of the memory array.

14. The information-handling system of claim 13, wherein the memory further comprises a second memory section, wherein the second memory section is operatively coupled to each processing element, and wherein the second memory section comprises:

a memory array;

a memory interface operatively connecting the memory array of the second memory section to each of the processing elements; and

a block transfer engine operatively coupled to the memory array of the second memory section, wherein the block transfer engine of the second memory section operates under command of one of the processing elements to transfer data from a memory location that cannot be addressed by the processing element to a memory location that can be addressed by the processing element.

15. The information-handling system of claim 13, wherein the first memory section further includes one or more I/O translation look-aside buffers, wherein each of the I/O translation look-aside buffers is operatively coupled to the memory array, wherein each of the I/O translation look-aside buffers is associated with a corresponding processing element, and wherein each of the I/O translation look-aside buffers has a second plurality of entries, each of the second plurality of entries being used to map an I/O address into a second memory array address of the memory array.

16. A method for transferring data in a memory comprising:

creating a block transfer command in a processor, wherein the block transfer command includes an amount of transfer data, a source transfer address, and a destination transfer address, wherein the source transfer address is a non processor-addressable memory address, and wherein the destination transfer address is a processor-addressable memory address;

routing the block transfer command from the processor to the memory; and

transferring the amount of transfer data from the source transfer address to the destination transfer address.

17. The method of claim 16, wherein the routing of the block transfer command includes processing the block transfer command on a first in first out basis with regard to a plurality of other commands.

18. An information-handling system comprising:

a memory; and

a plurality of processing elements, wherein each of the processing elements is operatively coupled to the memory,

wherein the memory includes transferring means for transferring data from a memory location in the memory that cannot be addressed by the processing elements to a memory location that can be addressed by the processing elements.

19. A system comprising:

a first information-handling system, the first information-handling system comprising:

a plurality of first processing elements; and

a first memory section, wherein the first memory section is operatively coupled to each of the first processing elements, and wherein the first memory section comprises:

a first memory array;

a first memory interface associated with the first memory array; and

a first block transfer engine operatively coupled to the first memory array, wherein the first block transfer engine is associated with each of the first processing elements through the first memory interface;

a second information-handling system, the second information-handling system comprising:

a plurality of second processing elements; and

a second memory section, wherein the second memory section is operatively coupled to each of the second processing elements, and wherein the second memory section comprises:

a second memory array;

a second memory interface associated with the second memory array; and

a second block transfer engine operatively coupled to the second memory array, wherein the second block transfer engine is associated with each of the second processing elements through the second memory interface; and

a communications channel connecting the first and second information-handling systems,

wherein the second block transfer engine transfers an amount of data from a first memory address in the second memory array to a second memory address in the first memory array over the communications channel.

20. The system of claim 19, wherein the first information-handling system further comprises one or more further memory sections, each of the memory sections substantially equal to the first memory section.

21. The system of claim 19, wherein the second information-handling system further comprises one or more further memory sections, each of the memory sections substantially equal to the second memory section.

22. The system of claim 19, wherein the first memory interface includes a FIFO, and wherein the FIFO accepts block transfer commands from one or more of the first processing elements and transmits the block transfer commands to the first block transfer engine.

23. The system of claim 19, wherein the second memory interface includes a FIFO, and wherein the FIFO accepts block transfer commands from one or more of the second processing elements and transmits the block transfer commands to the second block transfer engine.

24. The system of claim 19, wherein the first memory section of the first information-handling system further includes a processor translation look-aside buffer associated with each of the plurality of first processing elements, and wherein each processor translation look-aside buffer has a plurality of entries, each of the entries being used to map a processor address received from its associated processing element into a memory array address within the first memory array.

25. A method for transferring data in a system comprising:

creating a block transfer command in a processor of a first information-handling system, wherein the block transfer command includes an amount of transfer data, a source transfer address, and a destination transfer address, wherein the source transfer address is a first memory address of a first memory of the first information-handling

system, and wherein the destination transfer address is a second memory address of a second memory of a second information-handling system;

routing the block transfer command from the processor to the first memory of the first information-handling system; and

transferring the amount of transfer data from the source transfer address to the destination transfer address.

26. The method of claim 25, wherein the routing of the block transfer command includes processing the block transfer command on a first in first out basis with regard to a plurality of other commands.

27. A system comprising:

a first information-handling system comprising a first memory and a plurality of first processing elements, wherein each of the first processing elements is operatively coupled to the first memory;

a second information-handling system comprising a second memory and a plurality of second processing elements, wherein each of the second processing elements is operatively coupled to the second memory; and

means for transferring data from a first memory space of the first memory to a second memory space of the second memory.